ONE TIME EXIT SCHEME

USN | | | | | | | | | | |

10CS72

Seventh Semester B.E. Degree Examination, April 2018

Embedded Computing Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What are the characteristics of embedded computing applications? **(04 Marks)**

b. Why to use microprocessors and why not to use PC's for all embedded computing system? Explain in brief. **(08 Marks)**

c. Explain model train control system. List the basic set of requirements for the system. **(08 Marks)**

2 a. Explain format of ARM data processing instruction. **(04 Marks)**

b. Explain the following:
   i) Address translation for segment
   ii) Address translation for page **(08 Marks)**

c. With a neat diagram explain interrupt mechanism. **(08 Marks)**

3 a. With a neat diagram explain a bus with DMA controller. **(06 Marks)**

b. Explain any three input devices. **(06 Marks)**

c. Give a front panel of the alarm clock and also list requirements of alarm clock. **(08 Marks)**

4 a. Explain assembly, linking and loading in the compilation process. **(10 Marks)**

b. Explain the program optimization techniques. **(10 Marks)**

PART – B

5 a. Define RTOS. Explain with an example the Hard Real-Time and soft-Real Time. **(06 Marks)**

b. Give the differences between thread and process and also list the commonly available thread class libraries. **(06 Marks)**

c. Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds and priorities 0, 3, 2 (0-highest, 3-lowest priority) respectively enters the ready queue together. If a new process P4 with estimated completion time 6 ms and priority 1 enters the 'Ready' queue after 5 ms of execution of P1. Calculate the:
   i) Waiting time and turnaround time for each process.
   ii) Average waiting time and average turnaround time for processes.
   (Assuming there is no I/O waiting for the processes) in priority based scheduling algorithm. **(08 Marks)**

6 a. Explain the following:
   i) Shared memory communication
   ii) Message passing communication **(10 Marks)**

b. With respect to telephone answering machine, explain:
   i) System architecture
   ii) Component design and testing **(10 Marks)**

7 a. Explain typical bus transaction on the I^2C bus and also illustrate how I^2C encourages a data push-programming style. **(10 Marks)**

b. Define Distributed Embed System and explain the followings:
   i) Cross-bar network
   ii) Multi-hop network **(05 Marks)**

c. Explain the followings:
   i) Ethernet packet format
   ii) The internet service stack **(05 Marks)**

8 a. List the files generated on cross-compilation. Explain each file in brief. **(08 Marks)**

b. Explain features, advantages and limitations of simulator based debugging. **(06 Marks)**

c. Briefly explain target hardware debugging. **(06 Marks)**

* * * * *